IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS

Appellants:	John Donohue	**APPEAL BRIEF**
Serial No.	09/432,022	
Filing Date	October 29, 1999	
Group Art Unit	2631	
Examiner	Pankaj Kumar	
Attorney Docket No.	100.116US01	
Title: SYSTEMS AND METHODS FOR HOLDOVER CIRCUITS IN PHASE LOCKED LOOPS		

Table of Contents

1. Introduction....2
2. Real Party in Interest....2
3. Related Appeals and Interferences....2
4. Status of the Claims....2
5. Summary of the Amendments....3
6. Summary of the Invention....3
7. Issues Presented for Review....4
8. Grouping of Claims....4
9. Argument....4
   A. Rejections under 35 U.S.C. § 103(a)....4
      1. Applicable Law....4
      2. Analysis....5
10. Conclusion....9
11. Appendix 1 (The Claims on Appeal)....10

1. Introduction

On September 23, 2004, Appellant filed a notice of appeal from the final rejection of claims 1-3, 7, 23, 30 and 31 set forth in the Office Action mailed June 23, 2004. Three copies of this Appeal Brief are hereby timely filed on December 27, 2004, and are accompanied by a fee in the amount of $500.00 as required under 37 C.F.R. §1.17(c). A Petition for a one-month extension also accompanies this Appeal Brief, thereby moving the deadline to file the Appeal Brief from November 27, 2004 to December 27, 2004.

2. Real Party in Interest

The real party in interest in the above-captioned application is the assignee ADC Telecommunications, Inc.

3. Related Appeals and Interferences

There are no other appeals or interferences known to Appellant which will have a bearing on the Board's decision in the present appeal.

4. Status of the Claims

Claims 1-31 are pending in the application.

Claims 8-22 are allowed.

Claims 4-6 and 24-29 are objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1-3, 7, 23, 30 and 31 stand rejected under 35 USC § 103(a) as being unpatentable over Maddy (U.S. Patent No. 5,334,952) in view of Walley (U.S. Patent No. 6,606,364) and further in view of Momtaz (U.S. Patent No. 5,950,115).

5. Status of Amendments

An amendment after final has not been filed in connection with the final Office Action mailed on June 23, 2004.

6. Summary of the Invention

The present invention is directed to an improved phase locked loops that includes the capability to "hold" the output clock in a communication system at or very near the last output frequency before the loss of input data. This can prevent loss of data and communication with successive locations, or minimize disruption in communication, by avoiding rapid changes in data transmission rates.

In particular, an illustrative embodiment of the present invention (shown in FIG. 2 and described on page 4, line 24 – page 6, line 30 of the specification) includes a phase locked loop (200) which "holds" the output clock in a communication system at or very near the last output frequency before the loss of input data. The phase locked loop according to the teachings of the present invention includes a differential phase detector (202) that receives an input signal (204) and a feedback signal (206) and produces a differential output signal (208). An electronic selector circuit (210) is coupled to a differential output of the phase detector with an input that is responsive to a detected state of the input signal.

An operational amplifier based loop filter circuit (212) is provided in the phased locked loop. The electronic selector circuit provides the differential output of the phase detector at a pair of inputs (218A and 218B) to the operational amplifier. A voltage controlled oscillator (226) is coupled to an output of the operational amplifier and provides an output frequency (228) for the phased locked loop circuit. The electronic selector circuit is operable to control the input to the operational amplifier to hold an output frequency of the voltage controlled oscillator at a substantially constant frequency.

In the embodiment shown in FIG. 2, the electronic selector circuit includes a switch (220) which couples the pair of inputs together when a reference signal or input signal to the

phase detector is interrupted. In another embodiment (shown in FIG. 3 and described on page 7, line 1 – page 9, line 29), the electronic selector circuit includes a logic-based selector circuit (310) which holds the pair of inputs (318A and 318B) to an identical potential level when the input signal (304) to the phase detector (302) is interrupted.

7. Issues Presented for Review

The question presented in this Appeal is whether the Examiner erred in rejecting claims 1-3, 7, 23, 30 and 31 under 35 USC § 103(a) as being unpatentable over Maddy (U.S. Patent No. 5,334,952) in view of Walley (U.S. Patent No. 6,606,364) and further in view of Momtaz (U.S. Patent No. 5,950,115).

8. Grouping of Claims

Each of claims 1-3, 7, 23, 30 and 31 stands or falls on its own merits

9. Argument

A. Rejection of Claims 1-3, 7, 23, 30 and 31 under 35 USC § 103(a)

1. Applicable Law

35 U.S.C. § 103 provides in relevant part:

Conditions for patentability; non-obvious subject matter.

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

"The ultimate determination . . . whether an invention is or is not obvious is a legal conclusion based on underlying factual inquiries including: (1) the scope and content of the prior art; (2) the level of ordinary skill in the prior art; (3) the differences between the claimed

invention and the prior art; and (4) objective evidence of nonobviousness." *In re Dembiczak*, 175 F.3d 994, 998, 50 USPQ2d 1614, 1616 (1999) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966)).

When applying 35 U.S.C. §103, the claimed invention must be considered as a whole; the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention and a reasonable expectation of success is the standard with which obviousness is determined. *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2143

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. MPEP 2143 citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

2. Analysis

Claim 1 of the present application is as follows:

1. A phase locked loop circuit, comprising:

a differential phase detector that receives an input signal and a feedback signal and produces a differential output signal;

an electronic selector circuit having:

at least one first input coupled to the differential output signal of the phase detector; and

a second input that is responsive to a detected state of the input

signal;

a loop filter circuit having an operational amplifier, the operational amplifier having at least one amplifier input, wherein the electronic selector circuit provides the differential output signal of the phase detector to the amplifier input;

a voltage controlled oscillator coupled to an output of the operational amplifier and providing an output frequency for the phase locked loop circuit; and

wherein the electronic selector circuit is operable to control the amplifier input to hold the output frequency of the voltage controlled oscillator at a substantially constant frequency when the input signal to the phase detector is interrupted.

(Emphasis Added).

The Examiner, in the Office Action mailed January 21, 2004, conceded that Maddy (the base reference for this rejection) fails to teach "wherein the electronic selector circuit is operable to control the amplifier input to hold the output frequency of the voltage controlled oscillator at a substantially constant frequency when the input signal to the phase detector is interrupted" as is recited in claim 1 of the present application. The Examiner took the position that Momtaz teaches this. The Examiner concluded that it would have been obvious to one skilled in the art at the time of the invention to modify Maddy in view of Momtaz. In support of this conclusion, the Examiner asserted that Momtaz teaches, at column 10, lines 16-65, "holding the output frequency of the voltage controlled oscillator at a substantially constant frequency when the input signal to the phase detector is interrupted." (Office Action mailed January 21, 2004, paragraph 12). The Office Action explained that one would have been motivated to do so for the reasoning taught in Momtaz – "that when the link is interrupted, one loop is unable to compensate for the data frequency change exceeding the phase margin of the detector; thus, control has to be diverted to a second loop." (Office Action mailed January 21, 2004, paragraph 12).

Applicant respectfully submits the Examiner has failed to set forth a *prima facie* case of obviousness under 35 U.S.C. §103(a). The portion of Momtaz cited in the Office Action fails to

teach or suggest "wherein the electronic selector circuit is operable to control the amplifier input to hold the output frequency of the voltage controlled oscillator at a substantially constant frequency when the input signal to the phase detector is interrupted" as recited in claim 1 of the present application. The cited portion of Momtaz states, in relevant part, that:

> It will thus, be understood that a typical prior art-type phase lock loop based data recovery circuit comprises two separate loops; a phase and frequency loop and a phase only loop. After the PLL is locked to a known frequency by the phase and frequency loop, this loop is disabled and synchronization to an incoming data stream is performed in accordance with the phase only loop. The phase only loop ensures that the PLL output is in phase with the incoming data stream and if the input data frequency should drift slightly, the phase only loop is able to compensate for the drift so long as the data frequency change does not exceed the phase margin of the detector. However, if the drift is large enough or *if the incoming data link is temporarily interrupted, the phase only loop is unable to compensate and it must be disabled in its turn and control passed to the phase and frequency loop for reacquisition.*
>
> This dual-loop system requires complex monitoring and control circuitry to evaluate the operational state of the PLL and *in the event of a loss of velocity lock, disables the PLL for a significant period of time in order to reacquire lock prior to proceeding with data detection.* In accordance with practice of principles of the present invention, such complex monitoring control circuitry is no longer necessary and the operational state of a receiver PLL (28 of FIGS. 2 and 3) may be simply and efficiently evaluated against a known frequency reference. Frequency lock corrections are automatically applied whenever the receiver VCO frequency deviates from the reference by a pre-set amount, with the correction period typically comprising no more than 1.3 microseconds.

Momtaz, column 10, lines 35-64. Nowhere does the cited portion teach or suggest holding "the output frequency of the voltage controlled oscillator at a substantially constant frequency *when the input signal to the phase detector is interrupted*" as recited in claim 1 of the present application. The cited portion Momtaz does note that "if the incoming data link is temporarily interrupted, the phase only loop is unable to compensate and it must be disabled in its turn and control passed to the phase and frequency loop for reacquisition." However, this language does not teach or suggest holding "the output frequency of the voltage controlled oscillator at a

substantially constant frequency"; it merely states that the lock is reacquired "if the incoming data link is temporarily interrupted." *See, also,* Momtaz, column 3, line 62 – column 4, line 42, especially column 4, lines 27-32 (indicating that the output frequency of the VCO is not held constant when the "incoming data signal" is interrupted in such a system).

In the Final Office Action, the Examiner apparently argued that the references to a "known frequency" and a "known frequency reference" in the cited paragraphs from Momtaz set forth herein above (which references are underlined in the cited paragraphs) somehow describe holding "the output frequency of the voltage controlled oscillator at a substantially constant frequency when the input signal to the phase detector is interrupted" as recited in claim 1 of the present application. (See Final Office Action, paragraph 3). However, both such references are not describing an action that occurs "when the input signal to the phase detector is interrupted" as recited in claim 1 of the present application.

Moreover, Applicant respectfully submits that the Examiner has not provided an adequate motivation for one of ordinary skill in the art to make the proposed combination. As noted above, the motivation for the proposed combination provided by the Examiner is "that when the link is interrupted, one loop is unable to compensate for the data frequency change exceeding the phase margin of the detector; thus, control has to be diverted to a second loop." (Office Action mailed January 21, 2004, paragraph 12). However, the Examiner has failed to provide any basis for concluding that Maddy employs two such loops or that such a two-loop diversion scheme is at all relevant to a system that does not employ two such loops.

Accordingly, it is respectfully submitted that the Examiner erred in rejecting claim 1 of the present application under 35 USC § 103(a).

Claims 2, 3, and 7 ultimately depend from claim 1 and therefore, for at least those reasons set forth above with respect to claim 1, it is respectfully submitted that the Examiner erred in rejecting these claims.

Claim 23 recites, in part, "using the electronic selector circuit to control the amplifier input to hold the output frequency of the voltage controlled oscillator at a substantially constant

frequency when the input signal to the phase detector is interrupted".

The Examiner, with respect to this language from claim 23, used arguments similar to those used to reject claim 1 to reject claim 23. Therefore, for at least those reasons set forth above with respect to claim 1, it is respectfully submitted that the Examiner erred in rejecting claim 23.

Claims 30 and 31 ultimately depend from claim 23 and therefore, for at least those reasons set forth above with respect to claim 23, it is respectfully submitted that the Examiner erred in rejecting these claims.

10. Conclusion

Appellant has set forth reasons why the Examiner is incorrect in maintaining the rejections of the pending claims. Specifically, the Examiner has failed to set forth a *prima facie* case of obviousness under 35 U.S.C. §103(a). None of the references cited alone or in combination teach or suggest all the elements in the pending independent and dependant claims. Therefore, reversal of the Examiner's rejections is respectfully requested.

Respectfully submitted,

Date: 12/27/2004

Jon M. Powers
Reg. No. 43,868

Attorneys for Applicant
Fogg and Associates, LLC
P.O. Box 581339
Minneapolis, MN 55458-1339
T 612 332-4720
F 612 332-4731

Appendix 1

The Claims on Appeal

1. A phase locked loop circuit, comprising:

a differential phase detector that receives an input signal and a feedback signal and produces a differential output signal;

an electronic selector circuit having:

at least one first input coupled to the differential output signal of the phase detector; and

a second input that is responsive to a detected state of the input signal;

a loop filter circuit having an operational amplifier, the operational amplifier having at least one amplifier input, wherein the electronic selector circuit provides the differential output signal of the phase detector to the amplifier input;

a voltage controlled oscillator coupled to an output of the operational amplifier and providing an output frequency for the phase locked loop circuit; and

wherein the electronic selector circuit is operable to control the amplifier input to hold the output frequency of the voltage controlled oscillator at a substantially constant frequency when the input signal to the phase detector is interrupted.

2. The circuit of claim 1, wherein the electronic selector circuit de-couples the amplifier input from the differential output and holds the output frequency under an external command when the input signal to the phase detector is interrupted.

3. The circuit of claim 2, wherein the electronic selector circuit holds a current signal input to the operational amplifier when a reference signal to the phase detector is interrupted.

4. The circuit of claim 3, wherein the amplifier input includes a pair of amplifier inputs and wherein the electronic selector circuit holds a current signal input to the operational amplifier by

coupling the pair of amplifier inputs at the same potential.

5. The circuit of claim 4, wherein the electronic selector circuit includes a switch which couples the pair of amplifier inputs together when the reference signal to the phase detector is interrupted.

6. The circuit of claim 2, wherein the amplifier input includes a pair of amplifier inputs and wherein the electronic selector circuit includes a logic-based selector circuit which holds the pair of amplifier inputs to an identical potential level when the input signal to the phase detector is interrupted.

7. The circuit of claim 2, wherein the electronic selector circuit re-couples the amplifier input to the differential output of the phase detector when the input signal is restored.

8. A phase locked loop circuit, comprising:

a differential phase detector that receives an input signal and a feedback signal and produces a differential output signal;

an electronic selector circuit having:

at least one first input coupled to the differential output signal of the phase detector; and

a second input that is responsive to a detected state of the input signal;

a loop filter circuit having an operational amplifier, the operational amplifier having at least one amplifier input, wherein the electronic selector circuit provides the differential output signal of the phase detector to the amplifier input;

a voltage controlled oscillator coupled to an output of the operational amplifier and providing an output frequency for the phase locked loop circuit; and

wherein the electronic selector circuit de-couples the amplifier input from the differential output and holds the output frequency of the voltage controlled oscillator to a last received signal

from the differential output when the input signal to the phase detector is interrupted.

9. The circuit of claim 8, wherein the amplifier input includes a pair of amplifier inputs and wherein the electronic selector circuit includes a switch which couples the pair of amplifier inputs together to hold the last received signal as a current signal input to the operational amplifier when the input signal is interrupted.

10. The circuit of claim 8, wherein the amplifier input includes a pair of amplifier inputs and wherein the electronic selector circuit includes a logic-based selector circuit which holds the pair of amplifier inputs to an identical potential level to hold the last received signal from the differential output at the operational amplifier when the input signal to the phase detector is interrupted.

11. The circuit of claim 10, wherein the logic based selector circuit includes a pair of AND gates, each AND gate having an output coupled to one of the pair of amplifier inputs, wherein one input of each AND gate is coupled to the differential output, and wherein the other input of each AND gate is coupled to an external command signal source.

12. The circuit of claim 11, wherein the external command signal source provides a high potential to one input of each AND gate.

13. The circuit of claim 8, wherein the electronic selector circuit re-couples the amplifier input to the differential output of the phase detector when the input signal to the phase detector is restored.

14. The circuit of claim 8, wherein the output frequency of the voltage controlled oscillator provides the feedback signal to the differential phase detector.

15. A communication system, comprising:

a number of traffic cards having traffic inputs and traffic outputs;

a switching device coupled to the number of traffic cards; and

a synchronization source, coupled to the number of traffic cards, having a selector coupled to an external synchronization source and a controller, wherein the selector provides an input signal to a phase locked loop circuit, wherein the phase locked loop circuit is coupled to the controller, and wherein the phase locked loop circuit includes:

a differential phase detector that receives the input signal and a feedback signal and produces a differential output signal;

an electronic selector circuit having:

at least one first input coupled to the differential output signal of the phase detector; and

a second input that is responsive to a detected state of the input signal;

a loop filter circuit having an operational amplifier, the operational amplifier having at least one amplifier input, wherein the electronic selector circuit provides the differential output signal of the phase detector to the amplifier input;

a voltage controlled oscillator coupled to an output of the operational amplifier and providing an output frequency for the phase locked loop circuit; and

wherein the electronic selector circuit de-couples the amplifier input from the differential output and holds the output frequency of the voltage controlled oscillator to a last received signal from the differential output when the input signal to the phase detector is interrupted.

16. The system of claim 15, wherein the amplifier input includes a pair of amplifier inputs and wherein the electronic selector circuit includes a switch which couples the pair of amplifier inputs together to hold the last received signal as a current signal input to the operational amplifier under an instruction from the controller when the input signal is interrupted.

17. The system of claim 15, wherein the amplifier input includes a pair of amplifier inputs

and wherein the electronic selector circuit includes a logic-based selector circuit which holds the pair of amplifier inputs to an identical potential level, under an instruction from the controller, to hold the last received signal from the differential output at the operational amplifier when the input signal to the phase detector is interrupted.

18. The system of claim 17, wherein the logic based selector circuit includes a pair of AND gates, each AND gate having an output coupled to one of the pair of amplifier inputs, wherein one input of each AND gate is coupled to the differential output, and wherein the other input of each AND gate is coupled to an external command signal from the controller.

19. The system of claim 18, wherein the external command signal includes a high potential signal provided to one input of each AND gate.

20. The system of claim 15, wherein the electronic selector circuit re-couples the amplifier input to the differential output of the phase detector when the input signal is restored.

21. The system of claim 15, wherein the output frequency of the voltage controlled oscillator provides the feedback signal for the differential phase detector.

22. The system of claim 15, wherein the output frequency of the voltage-controlled oscillator further serves as a system clock to a number of system modules connected to the communication system.

23. A method for preventing data errors in a communication system, comprising:

coupling input data to a phase locked loop circuit, wherein the phase locked loop includes:

a differential phase detector that receives an input signal and a feedback signal and produces a differential output signal;

an electronic selector circuit having:

at least one first input coupled to the differential output signal of the phase detector; and

a second input that is responsive to a detected state of the input signal;

a loop filter circuit having an operational amplifier, the operational amplifier having at least one amplifier input, wherein the electronic selector circuit provides the differential output signal of the phase detector to the amplifier input; and

a voltage controlled oscillator coupled to an output of the operational amplifier and providing an output frequency for the phase locked loop circuit;

using the electronic selector circuit to control the amplifier input to hold the output frequency of the voltage controlled oscillator at a substantially constant frequency when the input signal to the phase detector is interrupted; and

using the electronic selector circuit to release control of the amplifier input so that the amplifier input follows the differential output when the input signal to the phase detector is restored.

24. The method of claim 23, wherein the amplifier input includes a pair of amplifier inputs and wherein using the electronic selector circuit to hold the output frequency of the voltage controlled oscillator at a substantially constant frequency includes using the electronic selector circuit to de-couple the pair of amplifier inputs from the differential output and hold the output frequency of the voltage controlled oscillator to a last received signal from the differential output when the input signal to the phase detector is interrupted.

25. The method of claim 24, wherein using the electronic selector circuit to de-couple the pair of amplifier inputs from the differential output includes using a switch to couple the pair of amplifier inputs together to hold the last received signal as a current signal input to the operational amplifier when the input signal is interrupted.

26. The method of claim 24, wherein using the electronic selector circuit to de-couple the pair of amplifier inputs from the differential output includes using a logic-based selector circuit to hold the pair of amplifier inputs to an identical potential level in order to hold the last received signal from the differential output at the operational amplifier when the input signal to the phase detector is interrupted.

27. The method of claim 26, wherein using a logic-based selector circuit to hold the pair of amplifier inputs to an identical potential level includes using a logic-based selector circuit having a pair of AND gates, coupling an output of each AND gate to one of the pair of amplifier inputs, coupling one input of each AND gate to the differential output, and coupling the other input of each AND gate to an external command signal source.

28. The method of claim 27, wherein using a logic-based selector having a pair of AND gates and coupling the other input of each AND gate to an external command signal source includes coupling the other input of each AND gate to a high potential.

29. The method of claim 23, wherein the amplifier input includes a pair of amplifier inputs and wherein using the electronic selector circuit to release control of the amplifier input so that the amplifier input follows the differential output includes using the electronic selector circuit to re-couple the pair of amplifier inputs to the differential output of the phase detector when the input signal is restored.

30. The method of claim 23, wherein the method further includes using the output frequency of the voltage controlled oscillator for providing the feedback signal to the differential phase detector.

31. The method of claim 23, wherein the method further includes using the output frequency of the voltage controlled oscillator as an output frequency for a system clock coupled to a number of system modules connected to the communication system.